and 9 is improper. Claims 8 and 9 have now been canceled but have been replaced by new claims 16 and 17 which are corresponding claims. Claim 16, like corresponding claim 18, is a linking claim and must be examined along with the claims to which it is linked. Thus, claim 16 should be examined along with claims 10-15 in accordance with the provisions of MPEP § 806.05(c). Claim 16 is the full apparatus counterpart of method claim 1 and is directed to apparatus for carrying out the steps of claim 1 wherein the steps are expressed in "means" form. It is respectfully submitted that the Examiner has not addressed this point and, in this regard, with respect to claims 8 and 9, the Examiner simply stated that these claims "are directed to Semiconductor Device which similar to the non-elected claim, i.e., claim 7 which is cancelled by applicants." This contention is not understood. In the first place, it is clear that claim 16 (which replaces claim 8) is not directed to a "semiconductor device" but rather is directed to an apparatus for carrying out the method of claim 1, as indicated above. Further, claim 16 is not "similar" to claim 7 in that, in contrast to claim 7, claim 16 is the direct "means" counterpart to method claim 10. Accordingly, it is respectfully requested that the Examiner reconsider the withdrawal of claims 8 and 9, insofar as applied to claims 16 and 17, and examine claim 16 along with claims 10-15. Further, as pointed out in the last response, if claim 16 is found to be allowable, claim 17 should be rejoined as a dependent claim based on claim 16.

With respect to the requirement for headings, new headings have been provided which generally correspond to those suggested. Although applicant is happy to comply, it is noted that headings are suggested rather than mandatory under 37 CFR 1.77(b). However,

Claim 1 has been objected to because of the form of indentation used. This form of indentation has been eliminated in the new claims presented.

Claims 1-6 have been rejected under 35 USC 112, second paragraph, as being "indefinite." As indicated above, claims 1-6 have been canceled and replaced by new claims 10-15. The objections to the claims have been kept in mind in drafting new claims 10-15 and it is respectfully submitted that these claims

as well as claims 16 and 17 are fully in accordance with the requirements of 35 USC 112.

Claims 1-6 have been rejected under 35 USC 102(b) as being "anticipated by" the Sawin et al patent. This rejection is made "based on prior art which reads on the interpretation the claim language of the instant application as best as understood by the Examiner." Insofar as this rejection is intended to apply to new claims 10-15 and new claim 16, the rejection is respectfully traversed.

The Sawin et al patent describes a measurement thickness method wherein the thickness of a layer is measured by interferometry between a plasma or light directed onto the engraved layer and a light resulting from the engraving reaction. Referring, for example, to Fig. 7 (or Fig. 5 or Fig. 8) of the reference, wherein a plot is provided of the interference minima and maxima as a function of time, it is evident that the oscillations stop when the entire 5,000 Angströms layer 313 has been etched, for an etching rate around 2,800 Angströms/min (see column 15, line 17 and column 16, line 45).

Considering the present invention, it is noted that the showing in Figure 3 is believed to be of help in understanding the invention and the differences thereof from the reference. Although the invention is obviously not limited to this embodiment, Figure 3 illustrates the amplitude of the light which is emitted during the engraving reaction. In particular, the peak of "plate no. 1" indicates that the SiN layer (the "underlying layer" as set forth in claim 10) has been reached at the time values prior to the peak value and that the first oxide layer has been reached at time values after the peak value. The peak value is reached when the engraving front reaches the boundary between the oxide layer and the SiN layer. This clearly has nothing to do with an interference maxima and minima diagram such as is disclosed in the reference.

According to the invention, light emitted during the engraving reaction is collected and the intensity thereof (the "amplitude" thereof as recited in claim 10) is measured in a spectral range comprising a characteristic emission wavelength of the underlying layer (i.e., the SiN layer in the preferred embodiment referred to above). This amplitude measurement can be carried out, for example, by using a

monochromator having a frequency centered around the SiN emission wavelength. No interference measurements are carried out in the method according to the present invention.

It is also noted that in the Sawin et al patent, there is no disclosure whatsoever of the use of a second, underlying layer in determining the thickness of a first, overlying layer during etching (engraving) thereof.

It is respectfully submitted that claims 10 and 16 clearly define over the Sawin et al reference. For example, there is no disclosure in the reference of an engraving reaction being applied to an underlying layer so as to generate a light emission having at least one spectral component, including the step of measuring the amplitude of light emitted during the engraving reaction in a selected spectral range comprising the at least one spectral component. Moreover, the passage in the Sawin et al reference at column 17, lines 60-68, indicates that for a wavelength of 404.7 nm (i.e., a wavelength near the SiN emission wavelength), the plasma light emission is not strong enough for interferometry to be observed. Thus, it is clear that one of ordinary skill in the art would find no teaching or suggestion in the Sawin et al reference of a method for providing an optical measurement of the thickness of a layer during an etching process based on simply measuring the plasma light emission in a spectral range around that of the underlying layer wavelength, as provided in accordance with the present invention.

Considering additional differences, the method for measuring thickness disclosed in the Sawin et al patent requires an external light source in the interferometry techniques used therein and also requires a CCD camera for measuring the interferometry patterns. In contrast, the thickness measurement according to the present invention is substantially simpler and merely requires means, such as a monochromator, for measuring the amplitude of emitted light in a chosen spectral range.

For the reasons set forth above, it is respectfully submitted that the method and apparatus of the present invention as claimed in claims 10 and 16 are both novel and non-obvious. Further, claims 11-15 are patentable for at least the

reasons set forth above in support of the patentability of claim 10. Accordingly, allowance of the application in its present form is respectfully solicited.

Respectfully submitted,

Date: February 12, 2003

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ATTACHMENT B

Marked Up Replacement Paragraphs

At the following locations, a marked up copy of the replaced paragraph is provided.

Page 1, the first paragraph:

FIELD OF THE INVENTION

The invention relates to a method and a device for controlling the thickness of a layer of an integrated circuit in real time during an engraving process.

BACKGROUND OF THE INVENTION

Page 3, lines 13-19:

SUMMARY OF THE INVENTION

The objective of this invention is to remedy the above-mentioned drawbacks of the prior art by eliminating the use of a sample silicon oxide deposition and by operating a method of measuring the thickness of a layer of an integrated circuit in real time during the production process, in particular when engraving this integrated circuit.

Page 4, lines 16-19:

BRIEF DESCRIPTION OF THE DRAWINGS

~~It~~The invention will be more readily understood from the description below and with reference to the appended drawings, of which, apart from figures 1a and 1b relating to the prior art:

Page 5, lines 6-10:

DETAILED DESCRIPTION OF THE INVENTION

Generally speaking, it should be pointed out that the method of measuring the thickness of a layer of an integrated circuit in real time may be applied as a means of measuring layers of any type during the process of engraving an integrated circuit of any type.